IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent Application No.: 09/998,469	Group Art Unit: 2814
Filing Date: November 29, 2001	Examiner: Peralta, Ginette
For: Barrier Layers For Protecting Metal Oxides From Hydrogen Degradation	Docket No.: 13176.403
Applicants: Solayappan et al.	Confirmation No.: 5686
	Attachment to Paper No.: 9

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that this correspondence, along with all papers referred to as being transmitted, are being facsimile transmitted to the Patent and Trademark Office Fax No. (703) 308-7724.

September 16, 2003 — Date

Elaine C. VonSpreckelsen — Elaine C. VonSpreckelsen

DECLARATION OF LARRY D. McMILLAN

I, Larry D. McMillan, hereby declare:

1. I am President and CEO of Symetrix Corporation at 5055 Mark Dabling Boulevard, Colorado Springs, Colorado, where I am involved in directing various research and business activities, which include integrated circuit manufacturing process development. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

2. I have worked for over thirty years as an integrated circuit process engineer. I have published more than a hundred papers and presentations on the subject of integrated circuit process engineering and have more than thirty issued patents in the field. A copy of my curriculum vitae with a partial list of my papers and patents is attached hereto.

3. Symetrix Corporation (Symetrix) is the assignee of the above-designated patent application (hereinafter, "the application").

4. I submit this Declaration to present to the Examiner, in an authenticated manner, facts concerning the relevance of the references cited in the Office Action dated June 16, 2003 (hereinafter, "the Office Action").

5. I have read the present claims of the application, the Office Action, and the

references cited by the Examiner, particularly, U.S. Patent Application Publication No. U.S. 2002/0038402 A1, published March 28, 2002, naming Kanaya (hereinafter "Kanaya"), and U.S. Patent No. 6,351,004 B1, issued February 26, 2002 to Shimada et al.. (hereinafter "Shimada").

6. The Shimada reference does not say that second insulating layer 8 prevents oxidation of source 3 and drain 4.

7. It is not inherently clear that an oxide second insulating layer 8 as disclosed in Shimada would protect against oxidation.

8. Shimada does not mention or discuss using second insulating layer 8 as a hydrogen barrier layer.

9. Even if second insulating layer 8 of Shimada were disclosed as a layer to protect against oxidation, there is no suggestion in Shimada or in the art in general that an element that protects against oxidation protects against hydrogen diffusion.

10. Metal-oxide hydrogen diffusion barrier layers comprising a material such as strontium tantalate, bismuth tantalate, and tantalum oxide, as claimed in independent claims 1 and 28 of the application, are generally electrically insulating.

11. Metal-oxide hydrogen diffusion barrier layers, such as strontium tantalate, bismuth tantalate, and tantalum oxide as claimed in independent claims 1 and 28 of the application, inhibit hydrogen diffusion by "gettering" hydrogen atoms, which reduce the functional oxides. Such metal-oxide materials do not protect well against oxidation.

12. Permittivity is directly related to the dielectric constant of a material by the equation

$$\varepsilon = K\varepsilon_0,$$

where ε is permittivity, K is a relative dielectric constant, and ε_0 is the permittivity of a vacuum.

13. It is well-known in the art that the insulating properties, the dielectric constant and thereby the permittivity of a metal oxide material, such as $SrTa_2O_6$,

decrease when the oxide is partially reduced by hydrogen, resulting in a non-oxide material replacing some of the oxide material.

14. It is also well-known in the art that a layer of metal oxide, such as $SrTa_2O_6$, that functions as a hydrogen diffusion barrier functions by "gettering" hydrogen atoms as they diffuse into the metal-oxide layer.

15. The hydrogen atoms reduce some of the oxygen atoms of the oxide material and thereby decrease the insulating characteristic and permittivity of the layer.

16. Accordingly, an insulating metal oxide, such as strontium tantalate ($SrTa_2O_6$), is useful in an integrated circuit either as a hydrogen barrier (as disclosed in the present application) or alternatively as an electrically insulating layer having high permittivity, but not as both.

17. If an insulating layer of metal oxide $SrTa_2O_6$ were used in an integrated circuit as a hydrogen diffusion barrier layer subjected to reductive process conditions involving reactive hydrogen atoms, some of the oxide would be reduced to a different, non-oxide compound and the resulting material would be unsatisfactory for its intended purpose of being a high-permittivity dielectric insulator.

18. The principle of operation of a metal oxide hydrogen barrier layer in accordance with the invention, such as strontium tantalate, is that some of the oxide is virtually sacrificed in its reaction with reactive hydrogen atoms during fabrication, and thereby has no functional role during actual operation of the integrated circuit.

19. In contrast, the principle of operation of a metal-oxide second insulating layer 8 in the Shimada reference is to function as a metal-oxide high-permittivity dielectric during actual operation of the integrated circuit.

20. Therefore, if second insulating layer 8 of Shimada were modified to serve as a hydrogen barrier layer in accordance with the present invention, at least a portion of the metal oxide would be reduced during fabrication processes, thereby changing the principle of operation of metal-oxide second insulating layer 8 of Shimada.

21. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements

and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Sept. 11, 2003
Date

Larry D. McMillan

Larry D. McMillan

EDUCATION

Ph.D. (Candidate)	University of Colorado at Colorado Springs
M.S.E.E.	Arizona State University, 1972
B.S.	Aquinas College, 1965 (physics and mathematics)

Michigan Technological University, 1986-1993
Adjunct Professor

EXPERIENCE

1988-Present — President and CEO
Symetrix Corporation

Corporate Management. Ferroelectric and other proprietary materials research and development, process and device development, program management and planning.

1984-1988 — Ramtron Corporation
Vice President (R&D) and Corporate Founder

Member, Ramtron Board of Directors. Research and development of ferroelectric memory devices and integrated circuits. Primary investigations of phase three potassium nitrate and other ferroelectric materials.

1982-1984 — Honeywell, Inc.
MOS Operations Manager

All MOS operations including wafer fabrication, maintenance, device engineering, process engineering, product engineering, test engineering, CAP/CAM, production testing and new process development. Member of Key Management Group (Corporate Level).

Manager, MOS Advanced Development

CAP/CAM development, CMOS process development, CCD TCL sensor process development, process transfers and long range planning activities. Developed and taught Operator and Technician Level IC Processing course (Honeywell Certificate Program).

MOS Process Engineering Manager

MOS production process engineering, maintenance, CCD process transfer from R&D to production, 3" to 4" wafer conversion, and advanced silicon gate MOS process development.

1980-1982 Stephenson Western, Inc.
Vice President

Engineering Consultant to the semiconductor industry. Computer modeling, fab design, UPDI water system design, process equipment selection, EPA regulations and hazardous chemical disposal. (Customer base included: Motorola, General Electric, Monolithic Memories, Fairchild, Signetics, Storage Technology, Intel and Mitel. (The firm was purchased by The Thomas Group.)

1979-1980 Storage Technology Corporation
Vice President and General Manager of Microtechnology Operations

Organized, staffed, designed and facilitized startup of semiconductor and thin film head and thin film media R&D and production facility.

1977-1979 National Cash Register (NCR) Corporation
Director of Engineering

All research, development and program management activities at the Colorado Springs NCR Integrated Circuit facility.

1976-1977 American Microsystems, Inc.
Manager, CMOS Process Engineering

All aspects of silicon gate CMOS process engineering, including process control and process development. VMOS and UMOS process development and transfer of NMOS process to Pocatello, Idaho facility. Developed and taught Operator and Technician Level Mathematics course.

1966-1976 Motorola, Inc.
Manager, Device Engineering (1975-1976)

Silicon gate NMOS fab device engineering and production process control. Established LPCVD silicon nitride and poly silicon as production processes in Austin, Texas facility.

Staff Scientist, Advanced Product R & D Labs (1973-1975)

Process development of 4K and 16K NMOS RAMS. Multi-level metal MOS development, spin-on metallic oxide development, and LPCVD poly silicon and silicon nitride development.

12 September, 2003

Manager, Linear IC Wafer Engineering (1973-1970)
Expanded Mesa, Arizona linear IC manufacturing capability from 2,000-2" wafers to 14,000-3" wafers per week. Linear device engineering, specification control, process control, wafer process engineering, linear process development, HIREL pilot line and wafer test. Developed and taught Engineering Level Process Engineering Classes (Motorola Certificate Program).

Engineering Manager, Product Engineering Liaison (1969-1970)
Safeguard Missile Program (secret). Beam lead processing.

Engineer, Motorola Advanced Pilot Line (1967-1969)
Photoresist, metalization, product development.

Engineer, Motorola Training Program (1966-1967)
MOS process development, C-V analysis, multi-layer metal, Epi, materials research, packaging.

12 September, 2003

Publications and Presentations

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H. Yoshimori, H. Watanabe, T. Mihara, H. Nakano, S. Hiraide, C.A. Paz de Araujo, & L.D. McMillan, "Process Integration for Y1 Capacitors with CMOS Devices",

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L. D. McMillan, "MOS C-V Techniques for IC Process Control", *Solid State Technology*, pp 605-610, September 1972

L. D. McMillan, "Semiconductor Process Newsletters", *Stephenson Western, Inc.*, (Published Monthly, 1980-1982)

L. D. McMillan and F. Stephenson, "Computer Model Analysis of Process Wafer Requirements and Associated Costs", *Microelectronics Measurement Technology Seminar*, San Jose, CA (18 March 1981).

C. A. Paz de Araujo, L. D. McMillan, and G. Rohrer, "Development of Advanced Non-Volatile Thin Film Ferroelectric Memories", UCCS Proposal, Funded, April 1984.

L. D. McMillan, "Rampac Development Program Status Review", *International Technology Symposium*, Sydney, Australia, 28 October 1985.

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L. D. McMillan, "Cubic Integration", Ramtron Technical Disclosure Level 2, *File No. 6, Document No. 018*, (1985)

C. A. Paz de Araujo, L. D. McMillan, R. B. Godfrey, and G. Rohrer, "High Speed (<100 ns) Non-Volatile Memory Using Ferroelectric Switching", *4th Australian Microelectronics Conference*, Sydney, Australia, May, 1985.

J. F. Scott, R. B. Godfrey, C. A. Paz de Araujo, L. D. McMillan, H. B. Meadows, and M. Golabi, "Device Characteristics of Ferroelectric Ceramic KNO_3 Thin-Film raw Memories", Proceedings of the *Sixth IEEE International Symposium on Applications of Ferroelectrics*, Lehigh University, Bethlehem, PA, June 8-11, 1986.

C. A. Paz de Araujo, J. F. Scott, R. B. Godfrey, and L. D. McMillan, "Analysis of Switching Transients in KNO_3 Ferroelectric Memories", *Applied Physics Letter*, Vol. 18, No. 21, May 26, 1986.

R. B. Godfrey, J. F. Scott, H. B. Meadows, M. Golabi, C. A. Paz de Araujo, and L. D. McMillan, "Analysis of Electrical Switching in Sub-Micron KNO_3 Thin-Films", *Ferroelectrics Letters*, Vol. 5, pp. 167-172, 1986.

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A. K. Kulkami, G. Rohrer, L. D. McMillan, and Adams, "Structural Properties Of Thin Film Memory Devices", *15th International Conference On Metallurgical Coatings*, San Diego, CA, April, 1988.

L. D. McMillan, "Ferroelectric Materials and Deposition Techniques", *Joint Industry and Government Conference on Ferroelectrics*, Colorado Springs, CO, September 13-14, 1988.

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L. D. McMillan, "New Space Age Electronic Materials", *Seminar On Electronic Materials*, Michigan Technological University, Houghton, MI, August 24, 1988.

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L. D. McMillan, C. A. Paz de Araujo, M. Scott, "High Dielectric Constant Materials and Processes for Advanced Multi-Layered PC Boards" *A Consultancy Report for Storage Technology Corporation*, May 30, 1991.

E. Fujii, Y. Uemoto, S. Hayashi, T. Nasu, Y. Shimada, A. Matsuda, M. Kibe, M. Azuma, T. Otsuki, G. Kano, M. Scott, L. D. McMillan, and C. A. Paz de Araujo, "ULSI DRAM Technology with $Ba_{0.7}Sr_{0.3}TiO_3$ Film of 1.3nm Equivalent SiO_2 Thickness and 10^{-9} A/cm^2 Leakage Current, presented at *International Electron Devices Meeting*, San Francisco, CA, December 1992.

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C. A. Paz de Araujo, L. D. McMillan, and J. F. Scott, "Processing of Ferroelectric Memories", *Materials Resource Society Symposium Proceedings*, Vol. 230, 1992.

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J. F. Scott, M. Azuma, E. Fujii, t. Otsuki, G. Kano, M. C. Scott, C. A. Paz de Araujo, L. D. McMillan, and T. Roberts, "Microstructure-induced Schottky Barrier Effects in Barium Strontium Titanate (BST) Thin Films for 16 and 64 mbit DRAM Cells", presented at *International Symposium on Applications of Ferroelectrics*, South Carolina, August 1992.

J. F. Scott, C. A. Paz de Araujo, L. D. McMillan, H. Yoshimori, H. Watanabe, T. Mihara, M. Azuma, T. Ueda, D. Ueda, and G. Kano, "Ferroelectric Thin Films in Integrated Microelectronics Devices", presented at the 25th *International Conference on Polar Dielectrics*, London, April 1992.

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J. F. Scott, C. A. Paz de Araujo, and L. D. McMillan, "Integrated Ferroelectrics", *Condensed Matter News*, Vol. 1, No. 3, pp. 16-20, 1992.

B. M. Melnick, M. C. Scott, C. A. Paz de Araujo, L. D. McMillan, and T. Mihara, "Anomalous Fatigue Behavior in Zn Doped PZT", *The Proceedings of the Fourth International Conference on Integrated Ferroelectrics*, Monterey, CA, p. 221, March 1992.

H. Yoshimori, H. Nakano, T. Milhara, H. Watanabe, C. A. Paz de Araujo, and L. D. McMillan, "A Low Density Ferroelectric RAM", *The Proceedings of the Fourth International conference on Integrated Ferroelectrics*, Monterey, CA, p 275, March 1992.

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J. D. Cuchiaro, M. C. Scott, C. A. Paz de Araujo, T. Mihara, and L. D. McMillan, "Switching Kinetics of Ferroelectric Fatigue Free Material", presented at *Fourth International Conference on Integrated Ferroelectrics*, Monterey, CA, March 1992.

L. D. McMillan, J. F. Scott, C. A. Paz de Araujo, invited paper, "Liquid-Source CVD of Ferroelectric Thin-Film Memories", *39th National Symposium, American Vacuum Society*, November 9-13, 1992.

B. M. Melnick, L. D. McMillan, and C. A. Paz de Araujo, "The Effect of "Excess Pb-Based Layered Capacitor Structures" on the Fatigue Characteristics of Ferroelectric Memories", April 15, 1992.

L. D. McMillan, "Deposition of Barium Strontium Titanate and Strontium Titanate via Liquid Source Chemical Vapor Deposition", abstract, *The First International Workshop on the Application of Ferroelectric Materials, Korea Advanced Institute of Science and Technology*, Taejon, Korea, October 21, 1993, p.91.

J. F. Scott, B. M. Melnick, L. D. McMillan, C. A. Paz de Araujo, and M. Azuma, "Dielectric Breakdown in High-ε Films for ULSI DRAMS", *Ferroelectrics*, 1993, Vol. 150, pp. 209-218.

T. Mihara, H. Yoshimori, S. Hiraide, H. Watanabe, Y. Kuroda, T. Takahashi, H. Nakano, C. A. Paz de Araujo, L. D. McMillan, and Y. Ishibashi, "Studies of Integrated Ferroelectric Thin Film Capacitors for Nonvolatile Memory Application", presented at *5th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, April 19-21, 1993.

T. Milara, H. Watanabe, H. Nakano, S. Hiraide, C. A. Paz de Araujo, and L. D. McMillan, "Process Integration for Y1 Capacitors with CMOS Devices", presented at the *5th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, April 19-21-1993.

C. A. Paz de Araujo and L. D. McMillan, "A New Material for Non-volatile Memory, Which Can Rewrite More Than 102 times, Was Developed and Measured", *Nikkei Electronics*, May 24, 1993, pp. 94-100 (Japanese text).

M. Azuma, E. Fujii, Y. Uemoto, S. Hayashi, t. Nasu, Y. Shimada, A. Matsuda, M. Kibe, T. Otsuki, G. Kano, M. C. Scott, L. D. McMillan, and C. A. Paz de Araujo, "ULSI DRAM Technology with High Dielectric Constant Materials", presented *at 5th International Symposium on Integrated Ferroelectrics*, Colorado Springs, CO, April, 1993.

J. F. Scott, M. Azuma, C. Z. Paz de Araujo, L. D. McMillan, M. C. Scott, and T. Roberts, "Dielectric Breakdown in High e Films for ULSI DRAMS: II Barium-Strontium Titanate Ceramics", *Matsushita Electronics Corporation 1993 Annual Report*.

L. D. McMillan, "Deposition of Barium Strontium Titanate and Strontium Titanate via Liquid Source Chemical Vapor Deposition", *Integrated Ferroelectrics*, Vol. 00, pp. 000-000, 1994.

M. Huffman and L. D. McMillan, "Liquid Source Misted Chemical Deposition: Technology Status and Recent Results", presented at the *2nd Pacific Rim Conference on Ferroelectric Applications*, Melbourne, Australia, November, 1994.

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